

## MOS FIELD EFFECT TRANSISTOR $\mu$ PA1716

### SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

### **DESCRIPTION**

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

### **FEATURES**

· Low on-resistance

 $R_{DS(on)1} = 12.5 \text{ m}\Omega \text{ TYP. (Vgs} = -10 \text{ V, ID} = -4 \text{ A)}$ 

RDS(on)2 = 17.0 m $\Omega$  TYP. (VGS = -4.5 V, ID = -4 A)

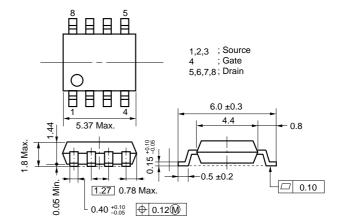
 $R_{DS(on)3}$  = 19.0  $m\Omega$  TYP. (Vgs = -4.0 V, Ip = -4 A)

- Low Ciss : Ciss = 2100 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
μ PA1716G	Power SOP8

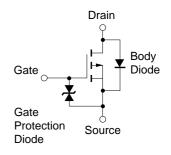
### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC)	ID(DC)	∓8	Α
Drain Current (pulse) Note1	D(pulse)	∓32	Α
Total Power Dissipation (T <sub>A</sub> = 25°C) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C

### **EQUIVARENT CIRCUIT**



- **Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
  - 2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 1.0 mm

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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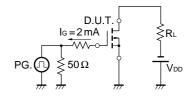
### ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -4.0 A		12.5	16	mΩ
	RDS(on)2	Vgs = -4.5 V, ID = -4.0 A		17	23	mΩ
	RDS(on)3	Vgs = -4.0 V, ID = -4.0 A		19	26	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	Vps = -10 V, Ip = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance	yfs	$V_{DS} = -10 \text{ V}, I_{D} = -4.0 \text{ A}$	7	14		S
Drain Leakage Current	IDSS	Vps = -30 V, Vgs = 0 V			-1	μΑ
Gate to Source Leakage Current	lgss	$V_{GS} = \overline{+} 20 \text{ V}, V_{DS} = 0 \text{ V}$			∓10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V V <sub>GS</sub> = 0 V f = 1 MHz		2100		pF
Output Capacitance	Coss			700		pF
Reverse Transfer Capacitance	Crss			300		pF
Turn-on Delay Time	td(on)	$ID = -4.0 \text{ A}$ $VGS(on) = -10 \text{ V}$ $VDD = -15 \text{ V}$ $RG = 10 \Omega$		30		ns
Rise Time	tr			150		ns
Turn-off Delay Time	<b>t</b> d(off)			120		ns
Fall Time	t <sub>f</sub>			76		ns
Total Gate Charge	Q <sub>G</sub>	ID = -8.0 A VDD = -24 V VGS = -10 V		40		nC
Gate to Source Charge	Qgs			6		nC
Gate to Drain Charge	Q <sub>GD</sub>			10		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 8.0 A, VGS = 0 V		0.8		V
Reverse Recovery Time	trr	IF = 8.0 A, Vgs = 0 V		45		ns
Reverse Recovery Charge	Qrr	$di/dt = 100 A/\mu s$		33		nC

### **TEST CIRCUIT 1 SWITCHING TIME**

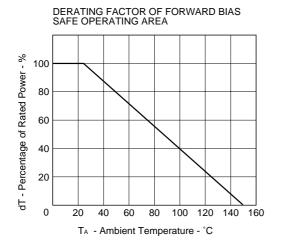
## $PG. \bigcap_{RG} R_{G} = 10 \, \Omega$ $V_{DD}$ $V_{GS} \bigvee_{Wave Form} V_{GS} \bigvee_{V_{GS} (on)} 90 \, \%$ $V_{GS} \bigvee_{Wave Form} 0 \, 10 \, \%$

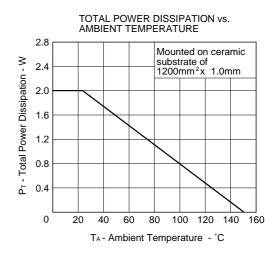
### **TEST CIRCUIT 2 GATE CHARGE**

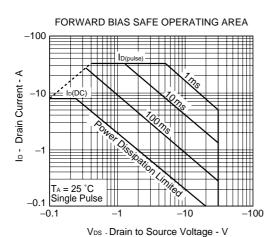




### TYPICAL CHARACTERISTICS (TA = 25 °C)

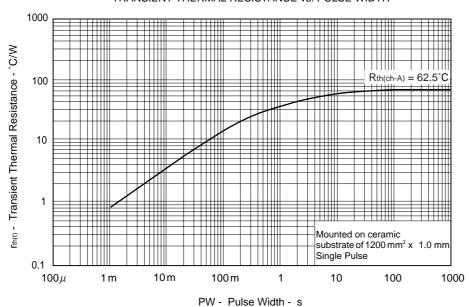






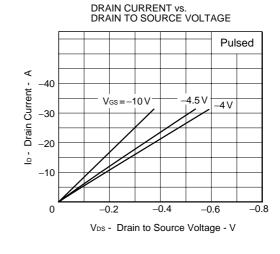
**Remark** Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 1.0 mm

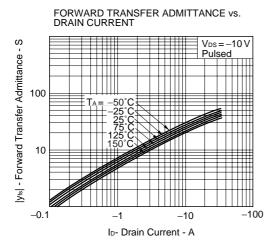
### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

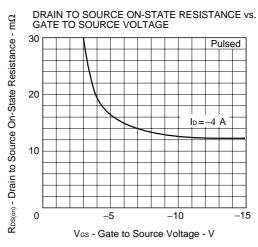


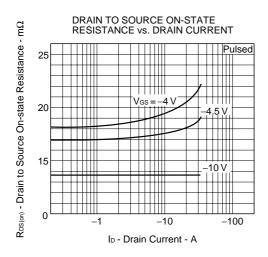
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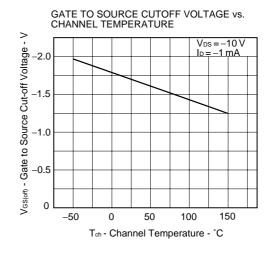
# FORWARD TRANSFER CHARACTERISTICS -100 -10 Ta = -25°C -25°C -25°C -150°C -150°C -0.1 Vos = -10 V Vos - Gate to Source Voltage - V

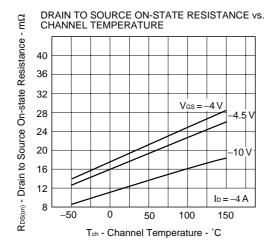


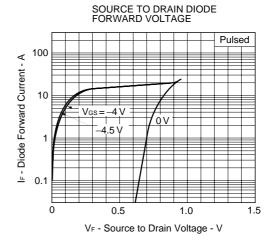


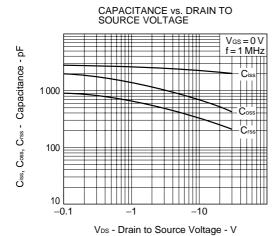


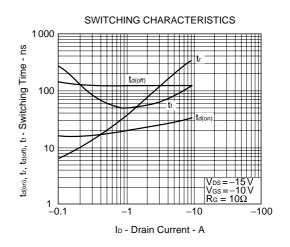


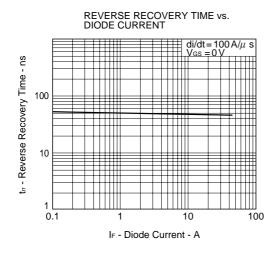


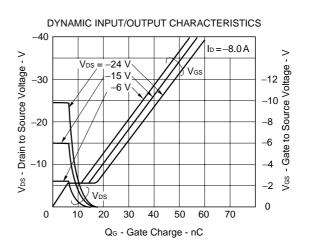












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